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EXAMINER	
KITOV, ZEEV	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,643	HIRAGA, NORIAKI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 3, 5 - 8, 10, 11, 15, 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5 - 8, 10, 11, 15, 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on March 26, 2004. Claims 1 and 5 are amended. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. The rejection follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 3, 5 – 8, 10, 11,15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tan et al. (US 5,991,134) in view of Shigemoto (US 5,923,570) and Otomo et al. (US 5,784,235).

Regarding Claim 5, Tan et al. disclose following elements of the Claim including a semiconductor integrated circuit device comprising a plurality of internal circuits arranged internally in a circuit-forming region (element 110 in Fig. 1 and 2), a plurality of external signal input/output circuits (implied by presence of the input bonding pads 120 in Fig. 1 – 3) having input protection circuits connected to input/output terminals outside the internal circuits (elements 130 in Fig.1 and 2).

It further discloses an active element in a first connection configuration (element 130 in Fig. 3) connected to the inter-circuit signal wire (line Vdd in Fig. 3), since line Vdd line in Fig. 3 and 10 being connected to the gates of different cells (elements Rg1 – RgN in Fig. 10) and carrying a signal of presence or absence of the power supply. It further discloses another element of an identical structure to the active element in the first connection configuration (elements 130 and 130A in Fig. 7 are identical and every bonding pad is connected to two protection elements on its right and left side). As to another active element protecting the active element in the first connection configuration, it is shown in Fig. 3 of Tan et al., wherein the additional ESD protection Circuitry (element 170) protects the internal circuit (element 110 in Fig. 3) from ESD events on power supply line Vdd. Tan et al. further disclose the gates of the active element in the second connection configuration being connected only to power lines (element 170 in Fig. 3 is the element with the second connection configuration). This element is further shown in Fig. 7 and indicated as 130A. However, it does not disclose the inter-circuit signal wire interconnecting the internal circuits.

Regarding Claims 1 and 5, Shigemoto discloses a clock wiring design having an inter-circuit wire (elements 18a, 18b and 18c in Fig. 1) interconnecting the internal circuits (elements A1, A2, B1, B2, C1, C2 in Fig. 1), which is not directly connected to the external signal input/output circuits. Internal circuit wires 18a, 18b and 18c are isolated from external environment by buffers 20a, 20b and 20c. It further discloses a plurality of internal circuits (elements A1, A2, B1, B2, C1 and C2 in Fig. 1). However it does not disclose the rest of the elements of the claim associated with an ESD

protection circuit. Both references have the same problem solving area, namely design of the integrated circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Tan et al. solution by adding the inter-circuit signal wire interconnecting the internal circuits according to Shigemoto, because as well known in the art, almost all digital circuits, with rare exception, use the clock signal, which is being generated at some location is transmitted to variety of cells.

As to the internal circuits having different power lines and the gates of the protection elements being connected to the power supply lines of the individual internal circuits, Otomo et al. disclose the internal circuits having different power lines (V21, V22, V23 and V2n in Fig. 12. More than that, the protection elements in Otomo et al. (diodes Pn1, Pn2 and P(n-1)n) are connected to the power supply lines of individual circuits. Therefore, in the Tan et al. circuit modified according to Otomo et al., the gates of the protection elements will be connected to the power lines of the individual circuits. Both references have the same problem solving area, namely protection of the semiconductor circuits against ESD. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Tan et al. solution by adding the feeding of the individual circuits from different power supplies according to Otomo et al., because as Otomo et al. state (col. 1, lines 14 – 24), reduction of power supply voltages in VLSI often requires to use different power supply voltages.

As per Claim 1, it differs from Claim 5 rejected accordingly by its limitation of plurality of other active elements. As was stated above, Tan et al. discloses both plurality of elements in the first and second connection configurations (elements 130 and 130A shown in Fig. 7).

Regarding Claims 2 and 7, Otomo et al. disclose a plurality of basic cells regularly arranged in repetition (shown in Fig. 12). As to the protection active elements in the first and second connection configurations, the Tan et al. solution modified according toi Otomo et al. will have the plurality of basic cells regularly arranged in repetition (shown in Fig. 12 of Otomo et al.), wherein each cell is protected by said the active elements in both the first and the second connection configurations allocated to some of the basic cells according to Otomo et al. A motivation for modification of the primary reference is the same as above.

Regarding Claims 3 and 8, Tan et al. disclose a substrate formed in a single chip, and the circuit-forming region is allocated to one surface of the substrate (shown in Fig. 7 – 10).

Regarding Claim 6, Tan et al. disclose a plurality of the active elements in the second connection configuration (elements 130A in Fig. 7). As to their position relative to the protected circuit, Examiner takes an Official Notice that positioning the ESD protection elements in close proximity to the protected circuit is a common practice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by placing both protection elements arranged in the first and the second connection configurations as

close as possible to the protected cell (surrounding the protected cell), because it reduces parasitic resistances and capacitances thus reducing a propagation delay in the ESD protection act.

Regarding Claim 10, as was stated above, Tan et al. and Otomo et al. disclose both protection elements arranged in the first and second connection configurations. Since Claims 5 and 10 do not disclose a structural difference between the first and the third connection configurations, they are interpreted as identical. The third connection configuration of Claim 10 fits exactly the definition of the protection element of Tan et al. as being connected to both a power line (Vdd in Fig. 3 and 9) and the inter-circuit signal wire, which is the same line Vdd (see above rejection of Claim 5). Otomo et al. disclose plurality of protection elements associated with each cell (diodes Pn1 – P(n-1)n in Fig. 12), thus satisfying limitation of plurality of protectin elements associated with each cell. By analogy, in the circuit of Tan et al. modified according to Otomo et al. the protection elements will include active elements, such as MOS transistors. Both references have the same problem solving area, namely protecting the semiconductor cirxcuits against ESD. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by adding the active element in a third connection configuration, because as Otomo et al. state (Fig. 9, col. 9, lines 49 – 59), in a case of plural power supplies the protection elements (diodes) should be connected between all power supply terminals (col. 12,line 57 – col. 13, line 32).

Regarding Claim 11, reciting a limitation of particular location of the protection element in the third connection configuration, Examiner takes an Official Notice that positioning the ESD protection elements in close proximity to the protected circuit is a common practice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by placing both protection elements arranged in the first and the second connection configurations as close as possible to the protected cell (surrounding the protected cell), because it reduces parasitic resistances and capacitances thus reducing a propagation delay in the ESD protection act.

Regarding Claim 15, Tan et al. disclose a plurality of the inter-circuit signal wires having different communication directions from each other interconnecting pair of internal circuits. The bonding pad 120 shown in Fig. 1 – 3 can be used for either transmission or reception of data signals between pairs of internal circuits. However, it does not explicitly disclose a pair of internal circuits communicating with each other. Otomo et al. disclose such pair of the circuits (elements 11 and 13 in Fig. 9). The circuits (elements 11 and 13 in Fig. 9 of Otomo et al.) have different communication directions (one transmits and the other receives the data); each of them has its own protection circuitry (elements 51, 52 and 31, 32 on the left side protecting element 11 and similar elements with the same numbers on the right side protecting element 13 in Fig. 9). When the pad 14 is connected to the pad 10, the output circuit will transmit signals to the input circuit. Examiner takes an Official Notice that such connections are often used in practice. In the circuit of Tan et al. modified according to a teaching of

Otomo et al. and having the output pad connected to the input pad, the input circuit protection is provided by the elements in the first and second connection configuration, while the output circuit protection is provided by the elements in the first and third connection configuration. Since no difference between the connections configurations have been provided in the claims, they are interpreted as being similar. The active element in the third connection configuration is independent of (not connected to) the active element in the second connection configuration. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by adding separate input and output circuits, because it is common in the art to have separate input and output pads (pins).

Regarding Claim 16, as was stated above, Tan et al. and Omoto et al. disclose the active elements in the second connection configuration and the third connection configuration being associated with the active elements in the first connection configuration. As to their positioning, Examiner takes an Official Notice that positioning the ESD protection elements in close proximity to the protected circuit is a common practice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Tan et al. solution by placing both protection elements arranged in the first and the second connection configurations as close as possible to the protected cell (surrounding the protected cell), because it

reduces parasitic resistances and capacitances thus reducing a propagation delay in the ESD protection act.

Response to Arguments

Applicant's arguments have been given careful consideration. Most of the arguments are now moot in view of new ground for rejection. However, some of them are to be addressed.

Examiner disagrees with the argument (page 2 of Remarks, lines 13 – 19), that "the element 170 does not protect the element 130". As is seen from Fig. 3 of Tan et al., element 130 is connected to both Vss and Vdd (through resistor R1). Therefore it is susceptible to damage caused by ESD event on line Vdd. Protection provided by element 170 across power lines is essential to prevent damage to element 130.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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